Measurements and Simulations of Cell Delays in ATM Switches

SABINE WITTEVRONGEL, DANNY DE VLEESCHAUWER, HERWIG BRUNEEL,
SMACS Research Group
Laboratory for Communications Engineering, University of Ghent
Sint-Pietersnieuwstraat 41, B-9000 Gent - Belgium
sw@telin.rug.ac.be

AXEL BRINKMANN,
Technology Centre for Mobile Communication
Stromerstrasse 5-7, D-90443 Nuernberg - Germany

REIN DE VRIES,
Seneca Advanced Communications,
Kluyverweg 2a, 2629 HT Delft - The Netherlands

Abstract. Within the RACE project EXPLOIT, traffic experiments are being performed on an ATM testbed, the EXPLOIT Testbed, which is situated in Basel. A subset of these experiments is described in this paper. Specifically, the network performance parameter cell delay, and especially the part due to queueing effects, is focused on. The aim of this paper is to compare the measurement results with the results of a generic simulation model based on renewal theory. It is shown that the simulation model predicts the delay histogram very well, but slightly underestimates the covariance over time of the delays.

1. INTRODUCTION

Over the past years various testbeds consisting of connected ATM switches and terminal adapters have been installed in Europe. One of these testbeds, the (RACE R2061) EXPLOIT Testbed (ETB), is situated in Basel. One of the main purposes of the EXPLOIT project is to determine the characteristic network performance parameters for traffic streams. Therefore experiments have been designed for investigating amongst others, cell delay, cell delay variation and cell loss. A description of the switch, terminal equipment and measurement equipment of the ETB can be found in [1]. This paper describes a subset of the experiments that were carried out on the ETB [2]. Specifically, the network performance parameter cell delay is focused on.

Cell delay can be split into three different components. Firstly, there is the processing delay, which can be understood as the amount of time it takes a cell to travel through the switch when there is no background load. This type of delay has a very small variance. A second contribution is the interface dependent delay, which is caused, for example, by the transition from SDH transmission to pure-ATM transmission, and vice versa. This delay has a small variance as well. Finally, there is the queueing delay which is due to the competition for output slots between cells of multiple traffic streams that are multiplexed within the switch. The queueing of cells is the major cause for the variability of the total cell delay. The interface and processing delay will be experimentally measured, and, where needed, their influence will be compensated for. Their explanation is beyond the scope of this paper. The queueing delay needs more attention and is investigated intensively in this paper.

Experimental results only depict a small sample of situations occurring in real life. Therefore it is essential to validate an underlying theoretical model, which enables to predict outcomes without performing further experiments. In this paper, the measured data are compared to the results of a generic simulation model, which uses a purely renewal theoretic approach. The aim of this paper is to verify whether this simulation model provides good predictions or not.

The remainder of the paper is organized as follows. In section 2, the conceptual set-up of the experiments is briefly described. Section 3 presents the generic simulation model. Section 4 gives the strategy behind the experiments. The results are reported and discussed in section 5. Three sets of experiments are considered in this paper. In the first, the influence of the foreground traffic is investigated. In the second and third, the background traffic is changed. Essential for the comparison of the measured delay histograms with the simulated delay histograms is the characterisation of the traffic
sources. Therefore the source characteristics of the used traffic streams were measured, and it is these that are used in the simulation model. The actual results are on the one hand depicted in an aggregated form (i.e. a histogram, in which time correlation of consecutive delays is lost), and on the other hand, in the form of the auto-covariance functions of consecutive delays. Finally, the main conclusions are summarized in section 6.

2. CONCEPTUAL SET-UP OF THE EXPERIMENTS

Fig. 1 illustrates the set-up considered in this paper. A foreground cell stream is routed through a switch to an output port. Several \((N - 1)\) background cell streams are fed into the switch and routed to the same output port. At this output port there is competition for slots on the output link, if two or more cells arrive at the same time at the output port. Hence, queueing occurs, and some cells are more delayed in favour of others. The histogram (which is an approximation for the probability mass function (PMF)) of the delay of foreground cells is under consideration. We measured this histogram on real switches with real sources and we will compare the measured histograms with histograms obtained from a simulation model.

In the following, various set-ups will be used. We will describe these by mentioning the switch under consideration, and specifying the number and characteristics of the sources. For the description of the hardware and software of the switches and the sources, we refer to [1]. Fig. 1 is merely a conceptual set-up. The real switch architecture can be very complicated.

![Fig. 1 - Conceptual set-up of the experiments.](image)

3. GENERIC SIMULATION MODEL

3.1. Assumptions

For the simulation model, several assumptions were made. Firstly, in an ATM switch there are usually a lot of different buffers and switching stages. A connection from an input port to an output port runs through several of these. In the simulation model, the switch is considered as a black box, and it is assumed that all queueing takes place in one single buffer at the output port. This buffer has a finite size \(S > 0\). Secondly, the switch is assumed to be fair. This implies that cells of different sources arriving in the same time slot are processed in a completely random order. Furthermore, the sources are modelled as renewal sources [3]. This means that a source is fully characterised by the PMF of the interarrival times (IAT) of the cells that it produces. All the sources are mutually statistically independent.

3.2. Buffer occupancy

Let us now define the random variable \(s_k\) as the buffer occupancy of the output buffer, i.e. the number of cells waiting in the output buffer including the cell in service if any, at the beginning of slot \(k\). Also, for each source \(n\) \((1 \leq n \leq N)\), let \(a_{n,k} (\geq 0)\) indicate the remaining IAT, i.e. the remaining number of slots until source \(n\) produces a cell, from the beginning of slot \(k\) onwards. If \(a_{n,k} = 0\), source \(n\) is producing a cell in slot \(k\); source \(n\) is silent during slot \(k\), if \(a_{n,k} > 0\). With these definitions, it is easily seen that knowledge of the value of the vector \((a_{1,k}, \ldots, a_{N,k}, s_k)\) is sufficient to determine the probability distribution of the vector \((a_{1,k+1}, \ldots, a_{N,k+1}, s_{k+1})\). Hence, the vector \((a_{1,k}, \ldots, a_{N,k}, s_k)\) constitutes an \((N + 1)\)-dimensional Markovian state description [3] of the system at the beginning of slot \(k\).

Let \(i_n\) indicate the IAT of the next two cell arrivals of source \(n\) at the beginning of slot \(k\). Then the following state equations can be established:

\[
\begin{align*}
a_{n,k+1} &= \begin{cases} 
i_n - 1 & \text{if } a_{n,k} = 0 \\ a_{n,k} - 1 & \text{if } a_{n,k} > 0 \end{cases} \\
\end{align*}
\]

(1)

i.e., if source \(n\) has produced a cell during slot \(k\), then the number of slots left until source \(n\) generates a cell at the beginning of slot \((k + 1)\) is equal to the source's (new) IAT minus 1; otherwise the remaining IAT of source \(n\) is decreased by one. Furthermore, let us denote the number of firing sources in slot \(k\) by \(e_k\). It is easily seen that

\[
e_k = \sum_{n=1}^{N} \delta(a_{n,k})
\]

(2)

where \(\delta(.)\) is the Kronecker delta function, i.e. \(\delta(x) = 1\) if \(x = 0\); \(\delta(x) = 0\) otherwise. Finally, the time evolution of the buffer occupancy is governed by the following equation:

\[
s_{k+1} = \min \left[ \max \left( s_k - 1, 0 \right) + e_k, S \right]
\]

(3)

3.3. Delay of the foreground cells

Let us consider a foreground cell \(C\) arriving in the output buffer during slot \(k\). Also, let \(u\) denote the number of cells waiting in the output buffer just before the arrival of cell \(C\). Then \(u\) is given by

\[
u = \min \left[ \max \left( s_k - 1, 0 \right) + f, S \right]
\]

(4)
where \( f \) is the number of cells arriving before the considered foreground cell \( C \) (in the same slot). This is a random variable depending on the total number of cell arrivals (i.e., \( e_k \)) during slot \( k \). If there are \( F \) arrivals in that slot, one of which is the foreground cell, then owing to the fairness assumption, the random variable \( f \) can take on the values 0, 1, ..., or \( F - 1 \), each with equal probability \( 1/F \), i.e. the foreground cell \( C \) can come first, second, ..., or \( F \)-th with equal probability. Remark that if \( u = S \), the arriving foreground cell finds the buffer full and is hence lost. If \( u < S \), the cell \( C \) effectively enters the output buffer and \( u \) equals the queueing delay \( d_u \) of \( C \). By means of eq. (4), the time evolution of \( u \) is calculated. Collecting the values of \( u \) of consecutive foreground cells, the simulated histogram \( h_u \) of \( u \) is built. The last bin in the histogram \( h_u \) (i.e. \( h_u(S) \)) is the cell loss ratio of the foreground source. The time evolution of the queueing delay of foreground cells immediately follows from the time evolution of \( u \). The simulated queueing delay histogram \( h_q \) is derived from \( h_u \) by renormalisation, i.e.

\[
h_q(j) = \frac{h_u(j)}{1 - h_u(S)}, \quad 0 \leq j \leq S - 1
\]

(5)

3.4. Simulation program

The time evolution of the above described Markov process has been simulated. The input to the simulation program is the buffer size \( S \), the number of sources \( N \), and for each source \( n \) \( \in \{1, 2, ..., N\} \) a PMF of IATs. The program allows 4 possible choices for this histogram:

a) for a geometric source of load \( \rho \),

\[
\text{Prob}[\text{IAT} = j] = \rho (1 - \rho)^{j-1}, \quad j \geq 1
\]

b) for a CBR source of load \( \rho \),

\[
\text{Prob}[\text{IAT} = K] = 1 - \alpha
\]

\[
\text{Prob}[\text{IAT} = K + 1] = \alpha
\]

where \( K \) is the largest integer value, that is smaller than or equal to the inverse load, i.e.

\[
K = \lfloor 1/\rho \rfloor
\]

and the parameter \( \alpha \) is chosen such that the mean IAT equals the inverse load. This leads to

\[
\alpha = \frac{1}{\rho} - K
\]

The above source is not exactly CBR, as there is no periodicity, but it is CBR in the renewal sense.

c) for an on-off source with peak load \( \rho \), average on-time \( \mu_{on} \) and average off-time \( \mu_{off} \),

\[
\text{Prob}[\text{IAT} = j] = (1 - \alpha) f(j - K) + \alpha f(j - K - 1), \quad j \geq K
\]

where \( K \) and \( \alpha \) are as under b), i.e. the IAT during an on-period equals \( K \) with probability \( (1 - \alpha) \) and \( K + 1 \) with probability \( \alpha \), and

\[
f(m) = \begin{cases} 
0 & m < 0 \\
1 - g & m = 0 \\
g(1 - r) r^{m-1} & m > 0 
\end{cases}
\]

Here \( g \) and \( r \) are given by

\[
g = \frac{1}{\rho \mu_{on} + 1} \quad \text{and} \quad r = 1 - \frac{8 \rho \mu_{on}}{\mu_{off}}
\]

For the on-off source it is assumed that the length of the off-period is geometrically distributed with parameter \( r \), where \( r \) is chosen such that the mean IAT equals the inverse load.

d) a list of IATs with their probability.

The first source \( (n = 1) \) is taken as foreground source (for which the delays are measured). The output of the simulation program is the histogram (or a trace, i.e. a time sequence of consecutive occurrences) of the queueing delays of the foreground cells.

4. EXPERIMENTS

4.1. Measurements

Experiments have been carried out on two ATM switches on the ETB, the LaTEX and the RUM [1]. The buffer sizes of the LaTEX and the RUM switches are 48 and 25 cells respectively. For the LaTEX switch, the interface type is SDH-framed ATM, whereas for the RUM switch, the interface type is pure ATM.

The measurable foreground traffic is generated in all experiments by the ATM-100 traffic generator [1]. The delay of each foreground cell is calculated by the traffic analyser by comparing the transmit timestamp put into the payload when the foreground cell leaves the ATM-100, with the receive timestamp given when the foreground cell is received back by the ATM-100. For the ATM-100, the minimal timestamp resolution is 1/4 of a slot (1) (at a bit rate of 155.52 Mbit/s).

The cell delay is measured for a large number of foreground cells and in this way the delay histogram is built. To achieve sufficient statistical significance, sample sizes of more than 10^7 cells are used.

(1) Because receive timestamps are given directly after the cell has been extracted from the SDH frame (when the output port is an ATM-in-SDH interface) and because the switch internal clock and the timestamp clock do not run perfectly synchronously, the delay may have a fractional value (which at first glance may look strange for a time-slotted system as ATM).
4.2. Processing and interface delay

When there is no background load on a switch, the foreground cells experience a so-called processing delay and interface delay. These delays have a small variance. This paper only deals with queuing delays. Therefore the following strategy is adopted. First, the delay histogram \( h_0 \) of the processing and interface delay \( d_0 \) is measured by switching off all background sources. Then, the delay histogram \( h_m \) is measured with all the background sources switched on. The delay \( d_m \) in this case consists of the processing and interface delay \( (d_0) \) and the queuing delay \( (d_q) \) in the switch, i.e. \( d_m = d_0 + d_q \). With the simulation model we only predict the queuing delay histogram \( h_q \). Therefore, we have to compensate by convolving it with \( h_0 \). Here we have assumed that the queuing delay \( d_q \) and the processing and interface delay \( d_0 \) are statistically independent. Hence, to see if our prediction \( h_q \) based on the simulation model is correct, we compare \( h_q \otimes h_0 \) with \( h_m \), where \( \otimes \) is the (discrete) convolution operator.

5. RESULTS

Three sets of experiments are considered. In the first, the influence of the foreground traffic is investigated. In the second and third, the influence of the traffic mix is studied by changing the background traffic. Some traffic sources are artificial, generated by test equipment; the others produce streams of cells with real data. Firstly, for each of the sets the exact traffic configuration is given and then, the corresponding results are stated.

5.1. The influence of the foreground traffic

5.1.1. Set-up and characterisation of the sources

Two similar set-ups are considered to study the influence of the foreground traffic: one on the LaTeX and one on the RUM. In these experiments an electrical ATM-SDH interface is used on the LaTeX switch. In both cases, the ATM-100 produces foreground cells. When the LaTeX is used, there are 3 artificial traffic generators as background sources: 2 NTUA-PCs [1], and the A8640 [1]. When the RUM is used, there are 4 background sources: one real traffic source, a VIDEO stream, and 3 artificial traffic generators, 2 NTUA-PCs and the A8643 [1].

The ATM-100 produces the foreground cell stream. Two cases of foreground cell streams are considered; they are both CBR:

- c1: 1 cell is followed by 99 idle slots. Its load is 0.01.
- c2: 1 cell is followed by 9 idle slots. Its load is 0.1.

All NTUA-PCs are set up to produce on-off traffic. The load during the on-period is measured as 0.344.

The average on-period is measured as 172.0 and the average off-period as 114.7. So, these sources produce an average load of about 0.206. The sojourn times of the on- and off-states are geometrically distributed.

The A8640 source is a VBR source with a measured load of 0.232. Its histogram of interarrival times was measured and is given in Fig. 2.

The VIDEO source produces a bit rate of about 34 Mbit/s (without the header information taken into account). Its histogram of interarrival times was measured and is given in Fig. 3. This source produces a nearly CBR stream with a load of 0.266.

The A8643 is set up as a CBR source: it produces a cell every 25 slots, and hence, has a load of 0.04.

For experiment c1, the total load is 0.654 when the LaTeX is used, and 0.728 when the RUM is used. For experiment c2, the total load is 0.744 on the LaTeX and 0.818 on the RUM.

5.1.2. Simulated versus measured histograms

In Fig. 4, the measured delay histogram \( h_m \) is compared with \( h_q \otimes h_0 \), i.e. the simulated queuing delay histogram \( (h_q) \), which was corrected with the measured
delay histogram of the processing and interface delay \( (h_p) \). It can be seen that in both the LaTeX-case and the RUM-case, the simulation results and the measurements are in fairly good accordance.

The peaks in the tail of the histogram for case \( c2 \) (i.e. at about delay 105 for the RUM) are due to buffer overflow in the finite buffers. For the LaTeX this effect does not occur as strong as for the RUM, since it has a larger buffer and the mean on-time of the PC sources is relatively small. For case \( c2 \), a cell loss ratio of \( 3.79 \times 10^{-3} \) was measured on the RUM. By means of the simulation program, a cell loss of \( 5.53 \times 10^{-3} \) is predicted. So, the simulation program can also be used to predict the cell loss ratio.

5.1.3. Simulated versus measured autocovariance functions

In the previous section, we have compared the measured and the simulated delay histograms. However, by aggregating the data into a histogram the information about the time evolution is lost. In this section, we take a look at the correlation of consecutive delays. In order to do so, first, a trace of the incoming foreground traffic in the measurement equipment has been made. Also, the simulated delay traces have been determined. In the measured delay traces the processing, interface and queuing delay are taken into account. In the simulated delay traces only the queuing delay is present. Next, the autocovariance functions \((ACF, \text{i.e. } ACF_d(l) = E[d(C) \cdot d(C + l)] - E[d(C)] \cdot E[d(C + l)])\) of the measured and simulated delay traces were calculated, and these are displayed in Fig. 5 (for the foreground source \( c2 \)). It can be seen that the ACF for the measured data lies above the ACF for the simulated data. For \( l = 0 \), i.e. for the variance of the delays, the difference is the (small) variance of the processing and interface delay. For larger values of \( l \), it seems that the simulation model slightly underestimates the measured covariance over time of the delays. This is due to the fact that we assumed the sources to be renewal sources, and neglected all correlation between consecutive IATs, which is only an approximation of the reality.

5.2. The influence of a geometric background load

5.2.1. Set-up and characterisation of the sources

In this set-up, all the sources are routed to an output port of the LaTeX switch. The interface used on the LaTeX is an optical ATM-in-SDH interface. The ATM-100 produces the foreground traffic. The background traffic is generated by 8 sources: 4 NTUA-PCs, 2 AUDIO streams, the A8643 and the A8640.

The ATM-100 is set up to produce a CBR stream. Its load is measured as 0.0104. All the NTUA-PCs are set up to produce CBR traffic. Their loads are measured as 0.00962. The AUDIO sources are also nearly CBR. Their loads are measured as 0.0102. The A8643 produces a CBR load measured as 0.0105.

The A8640 is set up to emulate a lot of low-load sources (each with a load of 0.00928, which is of the order of magnitude of the other sources), but since the A8640 is connected to only one port of the LaTeX,
### Table 1 - Histogram of interarrival times for the A8640: measured relative frequencies and theoretical probabilities

<table>
<thead>
<tr>
<th>Case</th>
<th>IAT</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>m1</td>
<td>Measured prob</td>
<td>0.7250</td>
<td>0.1888</td>
<td>0.0685</td>
<td>0.0154</td>
<td>0.0021</td>
<td>0.0002</td>
</tr>
<tr>
<td>m1</td>
<td>Theoretic prob</td>
<td>0.7238</td>
<td>0.1999</td>
<td>0.0552</td>
<td>0.0153</td>
<td>0.0042</td>
<td>0.0012</td>
</tr>
<tr>
<td>m2</td>
<td>Measured prob</td>
<td>0.8323</td>
<td>0.1415</td>
<td>0.0234</td>
<td>0.0026</td>
<td>0.0002</td>
<td></td>
</tr>
<tr>
<td>m2</td>
<td>Theoretic prob</td>
<td>0.8352</td>
<td>0.1376</td>
<td>0.0227</td>
<td>0.0037</td>
<td>0.0006</td>
<td>0.0001</td>
</tr>
<tr>
<td>m3</td>
<td>Measured prob</td>
<td>0.8657</td>
<td>0.1231</td>
<td>0.0107</td>
<td>0.0005</td>
<td></td>
<td></td>
</tr>
<tr>
<td>m3</td>
<td>Theoretic prob</td>
<td>0.8723</td>
<td>0.1114</td>
<td>0.0142</td>
<td>0.0018</td>
<td>0.0002</td>
<td></td>
</tr>
</tbody>
</table>

These sources are multiplexed inside the A8640. Since this is hard to model, we have chosen to model it as a source with geometrically distributed IATs, with a load as measured on an actual cell stream. This is justified by a theorem from renewal theory [3]. Table 1, in which measured relative frequencies are compared with theoretical probabilities, justifies this further. Three different cases are considered:

- **m1**: 78 CBR sources multiplexed, representing a load that was measured as 0.7238,
- **m2**: 90 CBR sources multiplexed, representing a load that was measured as 0.8352,
- **m3**: 94 CBR sources multiplexed, representing a load that was measured as 0.8723.

The total load on the LaTEX is 0.80358 for case m1, 0.91498 for case m2, and 0.95208 for case m3.

5.2.2. Simulated versus measured histograms

Fig. 6 compares the measured delay histogram $h_m$ and the corrected simulated queueing delay histogram $h_b \otimes h_n$. The figure shows that the simulation model predicts the measured results quite well. Note that the histogram $h_m$ in this figure is not the same as the histogram plotted in Fig. 4 a), since an electrical ATM-in-SDH interface was used in section 5.1, whereas an optical ATM-in-SDH interface was used in this section.

5.3. The influence of the background load of several sources

5.3.1. Set-up and characterisation of the sources

In this section, we consider two experiments on the LaTEX, r1 and r2, in which also real sources are used. The interface in these experiments is an optical ATM-in-SDH interface.

The ATM-100 produces the foreground cell stream. It is chosen to model a typical ISDN voice call (a 64 kbit/s CBR stream). Assuming AAL1 and taking the header
overhead into account it produces a load of 0.000464 (2). This value for the load has been verified by measurement.

There are 12 sources that load up the output port of the switch: 5 NTUA-PCs, the A8643, the 2 generators of the A8640, 2 VIDEO streams and 2 AUDIO streams.

The following sources remain the same in both experiments. 4 NTUA-PCs are set as on-off sources. Their measured characteristics are as shown in Table 2. The VIDEO was measured, and has a histogram of IAIs as displayed in Fig. 3. So, each VIDEO source produces a stream that is nearly CBR with a load of 0.266. The AUDIO sources are modelled as CBR sources with a load of 0.0102. The A8643 is set as CBR source and the load is measured as 0.0129.

Table 2 - Characteristics of the 4 NTUA-PCs set as on-off sources in the experiments r1 and r2

<table>
<thead>
<tr>
<th>PC</th>
<th>$\rho$</th>
<th>$\mu_{on}$</th>
<th>$\mu_{off}$</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0.0589</td>
<td>339.6</td>
<td>339.6</td>
<td>0.0295</td>
</tr>
<tr>
<td>10</td>
<td>0.0765</td>
<td>130.7</td>
<td>209.2</td>
<td>0.0294</td>
</tr>
<tr>
<td>23</td>
<td>0.0765</td>
<td>392.2</td>
<td>457.5</td>
<td>0.0353</td>
</tr>
<tr>
<td>26</td>
<td>0.0589</td>
<td>84.9</td>
<td>339.6</td>
<td>0.0118</td>
</tr>
</tbody>
</table>

The 3 remaining sources have different settings in both experiments. The 5-th NTUA-PC and the first generator of the A8640 are set to produce a CBR stream. The second generator of the A8640 is set so that a lot of small CBR sources are multiplexed inside the generator. As in section 5.2.1, we model this as a geometric source with a load measured on an actual cell stream. In Table 3, the loads for these 3 sources in both experiments are given. The total load is 0.777464 for experiment r1, and 0.875264 for experiment r2.

Table 3 - Load of the 5-th NTUA PC and the 2 generators of the A8640

<table>
<thead>
<tr>
<th>Source</th>
<th>Type</th>
<th>$r_1$</th>
<th>$r_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC 13</td>
<td>CBR</td>
<td>0.0472</td>
<td>0.0590</td>
</tr>
<tr>
<td>A8640(1)</td>
<td>CBR</td>
<td>0.0195</td>
<td>0.0325</td>
</tr>
<tr>
<td>A8640(2)</td>
<td>GEO</td>
<td>0.0390</td>
<td>0.1120</td>
</tr>
</tbody>
</table>

5.3.2. SIMULATED VERSUS MEASURED HISTOGRAMS

The measured delay histogram $h_m$ and the corrected simulated queueing delay histogram $h_q \otimes h_0$ are plotted in

---

(2) The load is the bit rate of the source divided by the link rate, corrected for the fact that in AAL1 only 47 of the 53 bytes of a cell are data bytes, i.e. (64/155520) * (53/47) = 0.000464.

Fig. 7 - Measured versus simulated delay histograms.

Fig. 7, for both experiments. Again, the figure reveals the good agreement between the generic simulation results and the measurements. The histogram $h_0$ in Fig. 7 differs from the one in Fig. 6 because another port was used on the LaTeX.

6. ACCURACY OF THE RESULTS

6.1. Accuracy of the measurements

Tables 4, 5 and 6 show the number of delays measured to build the histograms. In the first two sets of experiments ("c" and "m"), the delays of more than 10^6 foreground cells were measured. The reason that in the last set of experiments ("r") there are about one order of magnitude less measurements, is that the load of the measured stream is so low, that it would take too long to measure more than 10^6 cells.

Each bin of the histogram, i.e. each delay has a probability of occurring. Suppose the probability of the n-th bin is $p_n$. If we perform M experiments (and assume that

Table 4 - Number of delays measured in set of experiments "c"

<table>
<thead>
<tr>
<th>$h_0$</th>
<th>1.043676E+06</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h_m$: LaTeX; c1</td>
<td>1.935769E+06</td>
</tr>
<tr>
<td>$h_m$: LaTeX; c2</td>
<td>1.936638E+07</td>
</tr>
<tr>
<td>$h_m$: RUM; c1</td>
<td>1.572510E+06</td>
</tr>
<tr>
<td>$h_m$: RUM; c2</td>
<td>1.579259E+07</td>
</tr>
</tbody>
</table>

Table 5 - Number of delays measured in set of experiments "m"

<table>
<thead>
<tr>
<th>$h_m$: m1</th>
<th>4.591502E+06</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h_m$: m2</td>
<td>4.188781E+06</td>
</tr>
<tr>
<td>$h_m$: m3</td>
<td>3.778970E+06</td>
</tr>
</tbody>
</table>
Table 6 - Number of delays measured in set of experiments "r"

| \( h_0 \) | \( 1.65815E+05 \) |
| \( h_m; r1 \) | \( 3.21451E+05 \) |
| \( h_m; r2 \) | \( 7.75501E+05 \) |

these are statistically independent), the average number of hits for the \( n \)-th bin is \( M \, p_n \). The variance of this number of hits is \( M \, p_n \, (1 - p_n) \). So, the average value of the relative frequency of the \( n \)-th bin is \( p_n \) and its standard deviation is \( \sqrt{p_n \, (1 - p_n) / M} \). This means that the relative error on the measured relative frequency is higher, if the probability \( p_n \) is lower. In order to reliably measure a probability \( p_n \) with a relative error of the order of say \( 10^{-3} \), we have to perform \( M > 10^{2M} \, (p_n)^{-1} \) measurements. Notice that if we want the measured histogram to be accurate for one more order of magnitude, the number of required measurements (or measurement time) has to be two orders of magnitude larger.

From for example Fig. 4 a) (LaTEX; case c2) it can be seen that probabilities of the order \( 10^{-5} \) begin to show errors. Especially small probabilities are hard to measure correctly.

6.2. Accuracy of the simulations

For the accuracy of the simulations the same principles are valid. For the cases "c" and "m" \( 10^6 \) slots were simulated. In the cases "r" \( 10^9 \) slots were simulated. Since the delay is only measured for foreground cells, the number of delay measurements in each experiment varies. The average number of measured cells is the number of simulated slots multiplied by the load of the foreground cells. That is the reason why there are more slots simulated in experiment "r".

For the experiment on the LaTEX, with foreground source c2, 9 simulations have been performed with each time different seeds for the random number generators. The obtained histograms are displayed in Fig. 8. The load of the foreground traffic is 0.1 in this case, so that about \( 10^7 \) foreground cells make up the histogram. Therefore, errors are expected to start showing up at probabilities of about \( 10^{-5} \). This is also apparent from Fig. 8.

7. Conclusions

We have described a generic simulation model that has been used to predict experimental measurements on the ETB. Results show that the simulation model predicts the real behaviour quite well. The most important conclusion is that the assumptions made for the simulation model, (i.e. considering the switch as a black box with only one queue at the output port, assuming the sources to be renewal sources, and assuming the switch to be fair) are not too stringent to predict the queueing delay behaviour of an ATM switch.

Acknowledgements

Part of the work for this paper has been carried out within the RACE R2061 EXPLOIT project which is partially funded by the European Union. The authors would like to thank the partners in the EXPLOIT consortium, without their support this paper would not be possible. Thanks also go to the ASPA staff for their support on site while performing the experiments. The first and the third author wish to thank the Flemish Fund for Scientific Research (F.W.O. - Vlaanderen) for support of this research.

Manuscript received on October 2, 1995.

REFERENCES

[1] M. Potts: An overview of experience and achievements with the Explor Testbed. Submitted to ETT.