Concluding, the observed improvements were mainly due to the AR analysis, although spectral comparison and the non-stationarity coefficient might be useful at low SNRs. The AR-FIR filters needed a low number of taps, the LMS algorithm seems to be fast enough to capture slow variations of the noise characteristics and only one microphone is necessary. Moreover, the AR analysis might be used by noise cancelling techniques in speech recognition. Future work includes some heuristics to develop an endpoint detector, automatic threshold estimation, and the study of AR adaptation techniques.

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References

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Indexing terms: Asynchronous transfer mode, Queuing theory

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Introduction: In [1] a general relationship between the probability distributions of the delay of an arbitrary customer, and the system contents, during an arbitrary slot is derived under the most general conditions possible.

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Model and result: We consider a discrete-time queueing system with c servers and a deterministic service time of one slot for each customer. Owing to the discrete-time operation, time appears as being divided into fixed length slots S_t = (t_n, t_n+1), all customer arrivals and departures occur at the slot boundaries. Customers arrive according to a general arrival process and are queued for service according to a FIFO service discipline. The number of customers arriving at t_n is denoted as A_t. The buffer contents, i.e. the number of customers present, during slot S_t is denoted as U_t, and the delay of the jth customer C_t is denoted as D_t.

For any sample path of the queueing process, the average arrival rate λ is defined as:

\[
\lambda := \lim_{k \to \infty} \frac{1}{k} \sum_{i=1}^{k} A_t
\]

(1)

assuming the limit exists. Likewise, using the notation # to indicate the number of elements in a set, the distribution of the buffer contents U_t during an arbitrary slot can be characterised as:

\[
\Pr[U_t = n] := \lim_{k \to \infty} \frac{\#\{i | U_i = n, 1 \leq i \leq k\}}{k}
\]

and the delay distribution for an arbitrary customer is given by:

\[
\Pr[D_t = n] := \lim_{l \to \infty} \frac{\# \{ C_j \mid D_j = n, 1 \leq j \leq l \}}{l}
\]

(2)

again, under the assumption that these limits exist. A sufficient condition for this is that the limit λ in eqn. 1 exists and be strictly less than c.

In this letter we prove this regardless of the precise nature of the arrival process:

\[
\Pr[D_t = n] = \frac{1}{\lambda} \sum_{c=0}^{\infty} \binom{n-1}{c} \Pr[U_t = cn + p]
\]

(3)

where U_t is the system contents during an arbitrary mini-slot and D_t is the delay expressed in a number of mini-slots - of an arbitrary customer in the equivalent single-server queue.

First, we observe that during each slot the multiserver queue and the equivalent single-server queue serve the same customers. A customer that leaves the multiserver queue at t_n leaves the equivalent single-server queue at (t_n+c), where t_n+c is the arrival instant of the next customer in both queues. Therefore,

\[
D_t = n \Rightarrow \tilde{D}_t \in \{cn, cn - 1, \ldots, cn - c + 1\}
\]

so that for any l \in \mathbb{B}:

\[
\sum_{p=0}^{l} \# \{ C_j \mid \tilde{D}_j = n, 1 \leq j \leq l \} = \sum_{p=0}^{l} \sum_{c=0}^{\infty} \binom{n-1}{c} \Pr[U_t = cn + p, 1 \leq j \leq l]
\]

Fig. 1 Multiple server queue

In the equivalent single-server queue the number of ‘time-units’ is raised by a factor c, so that the load is \lambda c < 1. From [1] we can copy the result for the ‘equivalent’ single-server queue:

\[
\Pr[D_t = n] = \frac{c}{\lambda} \Pr[U_t = n]
\]

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Dividing by \( l \) and taking the limit for \( l \to \infty \) yields:

\[
\Pr[D = n] = \sum_{p=0}^{n-1} \Pr[D = cn - p] \quad n = 1, 2, \ldots
\]  

(4)

Secondly, consider a mini-slot during which the buffer contents in the equivalent single-server queue is \( n \), \( n \geq 0 \). The buffer contents in the actual multiserver queue, during the slot to which the mini-slot belongs to, is an element of \([n, n+1, \ldots, n+c-1]\). On the other hand, each slot with buffer contents that belongs to this set of values, contains exactly one mini-slot during which the buffer contents in the equivalent queue is \( n \). We thus obtain

\[
\#\{S_i|U_i = n, 1 \leq i \leq k\} = \sum_{p=0}^{n-1} \#\{S_i|U_i = n + p, 1 \leq i \leq k\}
\]

for all \( n = 1, 2, \ldots \). Dividing both sides by \( kc \) and taking the limit for \( k \to \infty \) we obtain

\[
\Pr[U = n] = \frac{1}{c} \sum_{p=0}^{n-1} \Pr[U = n + p]
\]  

(5)

A combination of eqns. 3, 4 and 5 readily gives the result stated in eqn. 2. This result allows the derivation of the mass-function of the delay of an arbitrary customer from the mass-function of the buffer occupancy during an arbitrary slot in the multiple-server queue. It is exactly the relationship found in [2], after a much more difficult reasoning, and under more restrictive conditions.

**Applicability:** The relationship in eqn. 2 is especially useful in the analysis of all kinds of queueing systems occurring in ATM networks, such as ATM multiplexers or output queues in ATM switches, in view of the constant length of the ATM cells (i.e. deterministic service times) and the usual FIFO serving rule in ATM.

In recent years many researchers have analysed the buffer contents distribution (and associated quantities such as cell loss ratio) in multiserver ATM queues with various types of bursty arrival models (such as on/off models, Markov modulated models, periodic arrival models, train arrival models, etc.) using various analysis techniques (i.e. analytical or semi-analytical approaches, numerical solutions, computer simulations). All their results can be transformed into corresponding results for the delay characteristics of these queues using the simple relationship established here. For instance, the following derivations required to obtain the delay performance of ATM switching elements, reported in [3] and [4], could have been completely avoided in this way.

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B. Vinck and H. Bruneel (Stochastic Modeling and Analysis of Communications Systems Research Group, Laboratory for Communications Engineering, University of Ghent, Sint-Pieterbrownstraat 41, B-9000 Gent, Belgium)

**References**


**Gallium arsenide pseudo-dynamic latched logic**

J.F. López, K. Esraghian, R. Sarmiento and A. Núñez

**Indexing terms:** Gallium arsenide, Logic circuits

A new GaAs logic family, pseudo-dynamic latched logic (PDLL), is introduced. Compared with traditional static GaAs logic families, PDLL allows complex gate design with less power dissipation. In addition, it overcomes problems associated with charge degradation in the storage nodes in dynamic logic gates, and operates at relatively high temperatures. PDLL is self-latched which leads to the possibility of implementing compact pipeline systems.

**Introduction:** In static GaAs logic families such as DCFL, SDCFL and SBFL, to obtain sufficient noise margin and performance, the load device must be correctly ratioed with a pull-down MESFET. This usually means that no more than two FETs in series can be used in the pull-down network, limiting the flexibility of the logic. Moreover, the circuit draws a constant current from the power supply producing a static dissipation which in some cases could limit the level of integration. These facts have generated an interest in mapping dynamic structures into GaAs in order not only to implement complex gates but also to reduce power dissipation.

The basic design aim in the implementation of dynamic logic gates is the storage of charge on circuit nodes which can be isolated temporarily from the remaining part of the circuit. GaAs technology presents the inherent problem of forward gate conduction which reduces the charge storage time in the isolated nodes. Most of the dynamic logic families presented have been designed in order to avoid this problem [1–3]. However they exhibit several disadvantages, such as low noise margins, inclusion of capacitor which results in area penalty and the use of several power supplies and even voltage references which pro duce variations in the performance of the circuits. More recent options have demonstrated performance improvement in the design of dynamic logic [4, 5].

**Fig. 1 Schematic diagram of PDLL inverter/non-inverter, and simulation results**

- **a** Schematic diagram
- **b** Simulation

**Pseudo-dynamic latched logic:** Owing to the high stability of the storage node, pseudo-dynamic latched logic (PDDL) overcomes the charge degradation problem associated with dynamic logic in gates. Moreover it allows the implementation of both true and complement functions in a single gate. Fig. 1 shows the structure for an inverting/non-inverting gate together with its simulation for a 2GHz clock frequency using a 1V power supply, thus dissipating only 150µW of power, which is ~20% of the power dissipated in a DCFL latch. This gate consists of an input stage where the logic function is implemented, and a static latch stage which is constantly refreshing the internal node. The circuit is synchronised by the clock signal which distinguishes precharge and evaluation phases. Precharge occurs when the clock is at high level (\( \Phi = 1 \)). During this time, \( T_i \) conducts to charge the internal node capacitance to a voltage which is limited by the forward conduction of the gate-to-source diode of the NOR gate. During the precharge period the output of the NOR is low because of the high logic level at the clock signal. When evaluation takes place (\( \Phi = 0 \)), inputs are not allowed to change, and the output of the NOR gate